Integrated CMOS Transceivers Using Single-Conversion Standard IF or Low IF RX For Digital Narrowband Cordless Systems

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Abstract — **This paper describes a 0.25um CMOS transceiver operating in the 902-928 Mhz ISM band for US Narrowband Digital Cordless Telephony. The DS9RF31 transceiver, intended for TDD systems, meets all specifications while providing a low cost, small die size solution. The transmitter uses open-loop FSK modulation and the receiver uses a single-conversion image-reject architecture followed by an IF chain and demodulator that provides output data to a baseband IC for further processing. One version of the chip uses a standard 10.7Mhz IF with discrete channel filters. A second version (DS9RF32) integrates the IF channel filter by using a low-IF of 1.36Mhz.**

I. Introduction

The main goal of the DS9RF31 was to successfully integrate a CMOS RF transceiver capable of replacing the company's current bipolar transceiver on the market, the DS9RF21. Consumer demands dictated that the transceiver do so at low die cost, power consumption, and external part count. In this paper, it will be shown that the DS9RF31 matches the DS9RF21, fabricated in a 12Ghz ft bipolar process, in all specifications including power consumption. In addition, the CMOS implementation exhibits two advantages. First, there is a significant shrinkage in die size due to the reduction in size of the synthesizer and digital blocks. Secondly, further integration of the transceiver is made possible through the design of a low-IF switched-capacitor channel filter that does not require any self-calibration circuitry.

II. Transceiver Architecture

Fig. 1 shows a block diagram of the DS9RF31. The DS9RF31 employs a 10.7Mhz IF using external channel filters while the DS9RF32 uses a 1.36Mhz IF with an integrated IF channel filter. The remaining IF blocks are identical except for the change in IF frequency. They include an IF limiter with RSSI, a quadrature discriminator, and a slicer. Both versions use an image-reject RF front-end consisting of an LNA, I,Q downconversion mixers, and a passive polyphase filter.

The transmitter consists of a synthesizer, a fully integrated VCO, and a 0 dBm TX buffer. The synthesizer must hop 10.7 Mhz (or 1.36 Mhz) between TX and RX frequencies each frame. During transmit, the PLL is opened and the VCO is directly modulated. The VCO operates at 2X the RF frequency to reduce RF pulling effects due to coupling between the TX output signal and the VCO. In addition, it allows for simple generation of the LO signals required by the synthesizer, receiver, and transmitter. A divide by 2 circuit creates accurate 0° and 90° LO signals for the IQ image-reject receiver. A second divide by 2 circuit conveniently provides one output for the synthesizer and the other output for the TX buffer.

The DS9RF31/32 transceiver architecture also integrates three additional functions. The T/R switch is eliminated by connecting the TX buffer output and LNA input together with a common external matching network. This connection is simplified by designing both the TX buffer and LNA as single-ended circuits. Also, a power ramping circuit ramps TX power on and off with a controlled time constant to keep spectral splatter below FCC limits. Finally, a 2.5V voltage regulator provides VCC for the entire IC, allowing it to operate with system supply voltages up to 3.6V without exceeding the voltage limits of the 0.25um CMOS process.

II. Circuit Implementations

A. Transmitter

The key specifications of the transmitter are set by the choice of an open-loop modulation scheme in a frequency-hopping protocol. The system protocol calls for a 128 kbps data rate and a 2ms TDD frame rate. During a transmit or receive time slot, there is a gap time of approximately 94us and a preamble of 125us to allow time for the synthesizer, demodulator, and slicer to settle. Thus, the synthesizer must be able to tune to any channel in the 902-928 Mhz ISM band and settle within 219 us. The frequency deviation of the FSK modulation is 60Khz peak. The integrated FM noise of the VCO must be < 4Khz rms in order not to degrade the S/N ratio of the radio link. Also, during the 1ms TX slot, the open-loop VCO

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frequency drift must be < 5 Khz in order not to degrade receiver bit error rate.

The fully integrated VCO consists of a cross-coupled NMOS differential pair, on-chip inductors, capacitively coupled tuning and modulation varactors, and an NMOS current source. The varactors are implemented using MOS transistors fabricated in an N well with source and drain tied together. The wide tuning range of this varactor compared to a standard pn varactor diode allows one to use a larger inductor in the tank for a given tuning range. The larger inductor translates into a larger impedance at resonance, requiring less current for a given voltage swing.

$$Z_{@res.}=Q*w_o*L \quad (1)$$

$$I_{vco}=V_{swing}/Z_{@res.}=V_{swing}/(Q*w_o*L) \quad (2)$$

(1) assumes that the inductor Q dominates overall tank Q.

CMOS VCO phase noise and current consumption are optimized by maximizing Q and inductance L, and by reducing 1/f noise from the bias and supply lines. The VCO uses the 2.5V regulated supply and its bias current is generated by on-chip biasing circuits. Both the regulated supply and the bias current are sources of 1/f noise which can be upconverted through the nonlinear response of the VCO. By low-pass filtering the bandgap voltage used by the regulator, and the gate of the NMOS current source; phase noise can be improved substantially. Fig. 2 shows the VCO closed loop phase noise with and without filtering. The 1/f corner frequency is 100Khz and has been attributed experimentally to the cross-coupled NMOS devices in the VCO core. This result is comparable to previously published results of standalone integrated VCO's. [1]-[2] The measured integrated FM noise of the VCO is 2.5Khz rms.

VCO frequency drift specifications were met through careful design of the charge pump and special ESD structures on the loop filter I/O that minimize leakage currents. The charge pump in Fig. 3 uses a current-steering architecture. During pumpup, switch Pu transfers 500uA from source P1 to the loop-filter while switch Pd transfers a dummy current to satisfy source N1. During pumpdown, switch Nd discharges the loop-filter while switch Nu provides a path for the dummy current. The voltage Vd is kept constant at Vcc/2 using a simple op-amp. It is important to prevent Vd from drifting significantly in order to maintain fast switching response and constant current pump. Measured open-loop frequency drift during a 1ms slot was < 1kHz.

The synthesizer consists of a 32/33 dual modulus prescalar, a 3-line serial interface, a 5-bit reference divider, a 9-bit main divider, a 5-bit auxiliary divider, a phase-frequency detector with dead-zone cancellation, and the charge pump. It uses a 4.096 Mhz crystal reference and a 227Khz comparison frequency. The prescalar consists of a divide by 2/3 core implemented with two differential OR flip-flops. The load is implemented with PMOS instead of the usual resistive load which eliminates the need for a constant current source and provides full CMOS rail-to-rail levels at its output. The remaining flip-flops are implemented in true-single-phase-clock (TSPC) to assure fast operation with minimal transistor count. A reference noise floor of < -80 dBc/Hz is achieved at the RF output frequency. A 30Khz loop bandwidth achieves a settling time of 170 us for a 10.7Mhz hop.

The TX buffer, shown in Fig. 4, consists of a cascade of two differential pairs which simultaneously provide gain, implement a 30dB gain step, and ramp TX power. MOS switches are used to provide the 30 dB digital gain step. Cascoded steering switches in the first differential pair, controlled by a ramp waveform, implement a 3 us ramp up and ramp down of the TX output power. Fig. 5 shows the power vs. time characteristics of the transmitter during turn-on and turn-off.

Following the buffer, a source follower drives a cascode amplifier that provides the 0 dBm output signal. The output match is left external so that a common matching network can be shared with the LNA, eliminating the T/R switch. During low-gain mode, the output buffer bias current is lowered to minimize power consumption.

B. Receiver

The receiver architecture uses an image-reject RF front-end to downconvert to the IF frequency. A high performance CMOS RF front-end, Fig. 6, has been designed using a novel patent pending topology that consists of an LNA, a passive single-ended to differential interface, and a differential V/I converter. [3] The LNA is a single-ended cascode amplifier. Recent publications on CMOS LNA's have utilized differential versions in order to reduce parasitic effects and improve common-mode noise rejection. [4]-[5] In this application and frequency range, a single-ended LNA has several advantages over a differential LNA. The single-ended LNA will have lower power consumption, lower noise figure, and will not require an external balun to interface to the antenna. Special care is taken to ensure proper isolation of the LNA from other circuit blocks. Separate bond wires are used for the common-source device ground and also to decouple the LNA VCC with an on-chip capacitor to ground.

The load of the LNA consists of a passive balun that converts the single-ended LNA output to a differential voltage swing across two grounded-source NMOS transistors. This interface eliminates the need for an active single-ended to differential stage that consumes power and dynamic range. It also provides a tuned resonance for the LNA load and DC biases the subsequent V/I converter through its center tap. The grounded-source NMOS transistors exhibit higher linearity than a conventional differential pair with current source and also take less voltage headroom, allowing the mixer gain to be maximized for a given supply voltage. The I and Q mixers use simple resistive loads at the IF port and are buffered with source followers to a 2 stage polyphase filter. This signal then drives an IF output buffer to interface to the IF channel filter. Overall, the RF front-end measured to the input of the IF channel filter has approximately 30 dB power gain and 4 dB noise figure. The front-end including IF buffers, LO buffers, and biasing consumes 20 mA.

In order to remove out-of-channel interferers from the desired signal before the IF limiter and demodulator, the IF signal is passed through a 200Khz BW bandpass filter. The DS9RF31 uses low cost readily available 10.7Mhz external ceramic filters. A cascade of two filters is used, with one filter placed before the IF amplifier and the other placed before the IF limiter. The second filter prevents the IF limiter from limiting on wideband noise generated in the IF amplifier stages and its own gain stages. The combined gain of the IF gain stages is over 90 dB.

In the DS9RF32, the 1.36Mhz bandpass channel filter is designed as a switched-capacitor circuit implementing a 6^{th} order LC ladder prototype. The filter center frequency and bandwidth are accurately controlled through a clock frequency (16.384Mhz) and capacitor ratios. This is an important advantage over active-RC implementations which require automatic tuning loops and replica stages to compensate for process RC variations. Table 2 shows the measured response of the bandpass filter. A total filter capacitance of approximately 200pF is used to reduce noise contributions that can degrade overall receiver noise figure. The large capacitors require high bandwidth opamps to settle during each clock phase, leading to a filter current consumption of 7mA. Capacitors are initially scaled to keep filter node voltages constant and capacitor ratios reasonable. A final capacitor scaling is then done to optimize settling behavior of the opamps. Measured results on the DS9RF32 receiver show 5 dB overall NF and –25 dBm IIP3. The complete IF filter including anti-aliasing filter, postfilter, and biasing consumes 10 mA and takes 0.8 mm^2 of die area.

The IF signal is demodulated by a quadrature-type FM discriminator with an external resonant tank. The discriminator uses digital XOR gates to implement a mixer used as a phase detector. The output of the discriminator is lowpass filtered and applied to a slicer. During the design, it was found that CMOS switching transients in the digital gates of the discriminator and slicer caused broadband noise generation that degraded noise figure. By sizing devices properly to slow down the switching transients, this problem was solved.

III. SUMMARY OF RESULTS

Table 1 summarizes measured results for the DS9RF31 transceiver compared to the DS9RF21 bipolar transceiver. The CMOS transceiver consumes 15% less current than the bipolar transceiver in all modes of operation- TX, RX, and standby.

TABLE 1: DS9RF31 Radio Performance

Specifications	DS9RF31 (CMOS)	DS9RF21 (Bipolar)
VCO Phase Noise (10kHz,100kHz offset)	-70 dBc/Hz, -100 dBc/Hz	-78 dBc/Hz -98 dBc/Hz
Closed Loop Synthesizer Noise Floor	-82 dBc/Hz	-72 dBc/Hz
TX Output Power (LNA,TX share match)	2 dBm	2 dBm
TX Open Loop Drift(1ms)	230 Hz	500 Hz
NF (LNA,TX share match)	5 dB	4.8 dB
Sensitivity (BER=1E-3)	-105.5 dBm	-106.5 dBm
Die Area	6.5 mm^2	9 mm^2

IV. CONCLUSION

This paper demonstrates a low cost, compact CMOS RF solution for US900 NB Digital Cordless Telephony. High performance and integration are achieved through architectural choices and innovative RF design. A second version of the IC demonstrates a low-IF switched-capacitor bandpass filter that achieves further integration.

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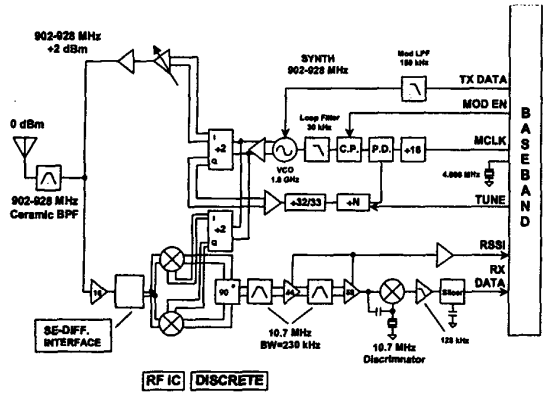

Fig. 1 DS9RF31 Block Diagram

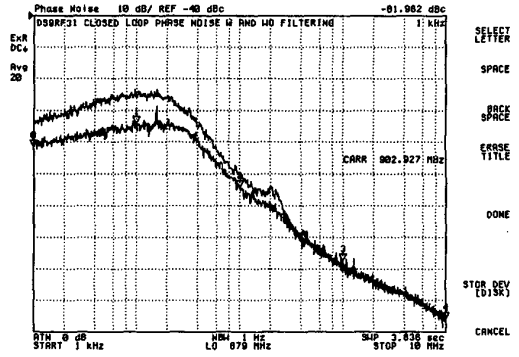

Fig. 2 Closed Loop Phase Noise with and without filtering

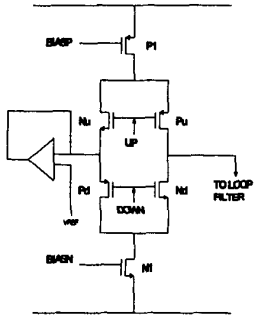

Fig. 3 Charge Pump

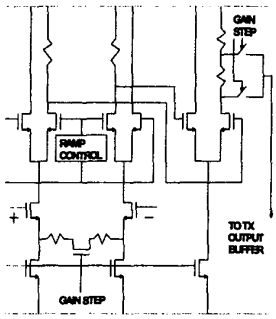

Fig. 4 TX Buffer

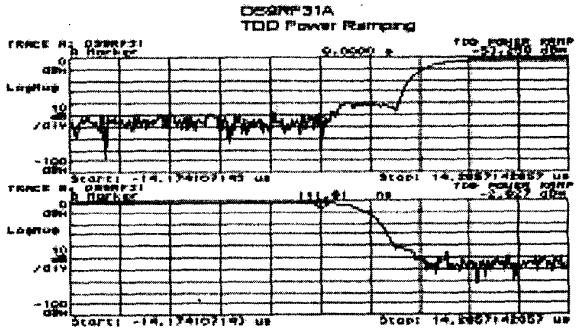

Fig. 5 TX Power vs. Time (Turn-on and Turn-off)

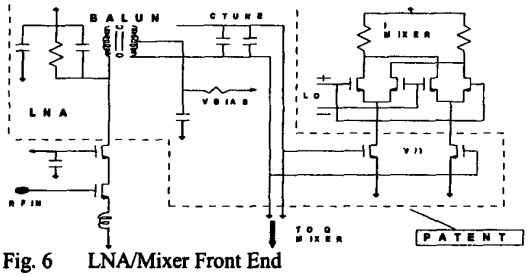

Fig. 6 LNA/Mixer Front End

TABLE 2: 1.36Mhz Bandpass Filter

Filter Performance	Measured	Spec
6 dB BW	200Khz	200Khz
Atten. +/- 100Khz	-6 dBc	-6 dBc
Atten. +/- 200Khz	-21 dBc	-15 dBc
Atten. +/- 300Khz	-33 dBc	-30 dBc
Atten. +/- 400Khz	-42 dBc	-40 dBc
Atten. +/- 500Khz	-47 dBc	-45 dBc
IIP3	+23 dBm	+25 dBm